CLAIMS:

1. An electric device comprising:

- a semiconductor body (1) comprising a group IV semiconductor material having a surface (2),
- a nanostructure (3) of a III-V semiconductor material,

characterised in that the nanostructure is a nanowire (3) being positioned in direct contact with the surface (2) and having a first conductivity type, the semiconductor body (1) having a second conductivity type opposite to the first conductivity type, the nanowire(3) forming with the semiconductor body a pn-heterojunction (4).

2. An electric device as claimed in Claim 1, characterised in that the III-V material is a diffusion source (5) of dopant atoms into the semiconductor body.

3. An electric device as claimed in Claim 2, characterised in that the diffusion source (5) contains the group III atoms and/or the group V atoms from the III-V material.

4. An electric device as claimed in Claims 1 or 3, characterised in that there is a region (6) in the semiconductor body in direct contact with the nanowire (3), which has the same conductivity type as the nanowire.

5. An electric device as claimed in Claim 2, characterised in that the III-V material comprises an excess of the group III atoms and/or the group V atoms of the III-V material, which excess atoms form the dopant atoms in the semiconductor body.

6. A device according to claim 1, characterised in that the nanowire is in epitaxial relationship with the semiconductor body and the materials have a mutual lattice mismatch.

7. A device according to claim 2, characterised in that the resistance between the nanowire (3) and the semiconductor body (1) is below $10^{-5}$ Ohm $cm^2$.

8. A device according to claim 1, characterised in that a lattice mismatch between the semiconductor body (1) and the nanowire (3) is smaller than 10%.

9. A device according to claim 1, characterised in that the nanowire (3) is a substantially single-crystal nanowire.

10. A device according to claim 1, characterised in that a plurality of nanowires are arranged in an array (7).

11. A method of forming a pn-heterojunction, the method comprising the steps of:

- forming a nanostructure (3) of a second semiconductor material on a surface (2) of a semiconductor body (1) of a first semiconductor material,

the first semiconductor material comprising at least one element from group IV of the periodic system and the second semiconductor material being a III-V material,

characterised in that the nanostructure is a nanowire (3) grown on the surface (2) of the semiconductor body (1) and receiving a first conductivity type, the semiconductor body having a second conductivity type opposite to the first conductivity type, the nanowire (3) forming with the semiconductor body (1) a pn-heterojunction (4).

12. A method as claimed in Claim 11, characterised in that the nanowire of III-V semiconductor material is used as a diffusion source (5) of dopant atoms into the semiconductor body.

13. A method as claimed in Claim 12, characterised in that group III atoms and/or the group V atoms from the III-V material are the dopant atoms.

14. A method as claimed in Claim 11, characterised in that the nanowire is grown in epitaxial relationship with the semiconductor body.

15. A method as claimed in Claim 14, characterised in that the nanowire is grown according to the vapour-liquid-solid (VLS) growth method.

16. A method as claimed in Claims 14 or 15, characterised in that an excess of the group III atoms and/or the group V atoms are grown in the III-V semiconductor material, which excess atoms are diffused into the semiconductor body.

17. A method as claimed in Claims 14 or 15, characterised in that at least one element of the periodic system is incorporated in the III-V semiconductor material of the nanowire, which element is diffused into the group IV semiconductor material, forming an n-type or p-type dopant atom.

18. A method as claimed in Claims 11 to 17, characterised in that the dopant atoms form a region (6) in the semiconductor body in direct contact with the nanowire (3).

19. A method as claimed in Claims 11 or 12, characterised in that the III-V semiconductor material of the nanowire is heated above 600 °C.

20. A method as claimed in Claim 19, characterised in that the nanowire is embedded in a dielectric before heating.

21. A method as claimed in Claim 12 or 19, characterised in that the nanowire is selectively removed after being used as diffusion source (5).